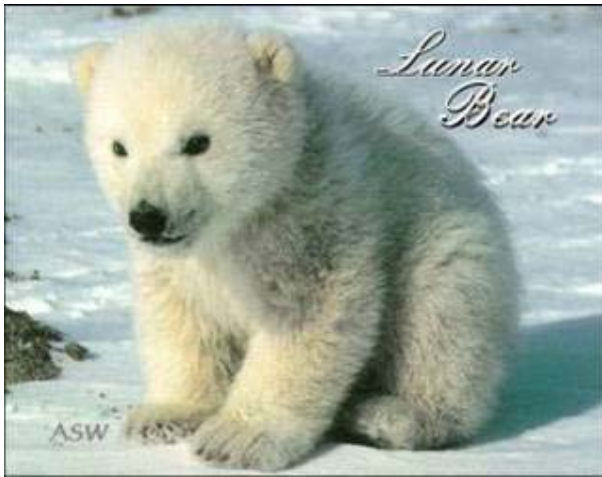


Lunar2 Bear

MS-7415 Version 0B



CPU:

Intel Conroe/Conroe-L/
YorkFiele/Wolfdale - 65W CPU
(FSB1333/1066/800/533)

System Chipset:

Intel BearlakeQ35 - GMCH (North Bridge)
Intel ICH9 DO (South Bridge W/ AMT)

On Board Chipset:

BIOS - SPI FLASH
HD Audio - Realtek ALC262 C2
LPC Super I/O : SMSC SCH5617
Gigabit LAN - Intel Nineveh 82566
Clock GEN - ICS9LP505-1
TPM - SLB 9635 TT1.2

Main Memory:

DDR II(800/667)*2 (Up to 4GByte)

Intersil PWM:

Controller - Intersil 6326 3Phase

Expansion Slots:

PCI-E[X16] Slot *1
Riser Slot : (PCI*1/PCI-E[X1]*1)

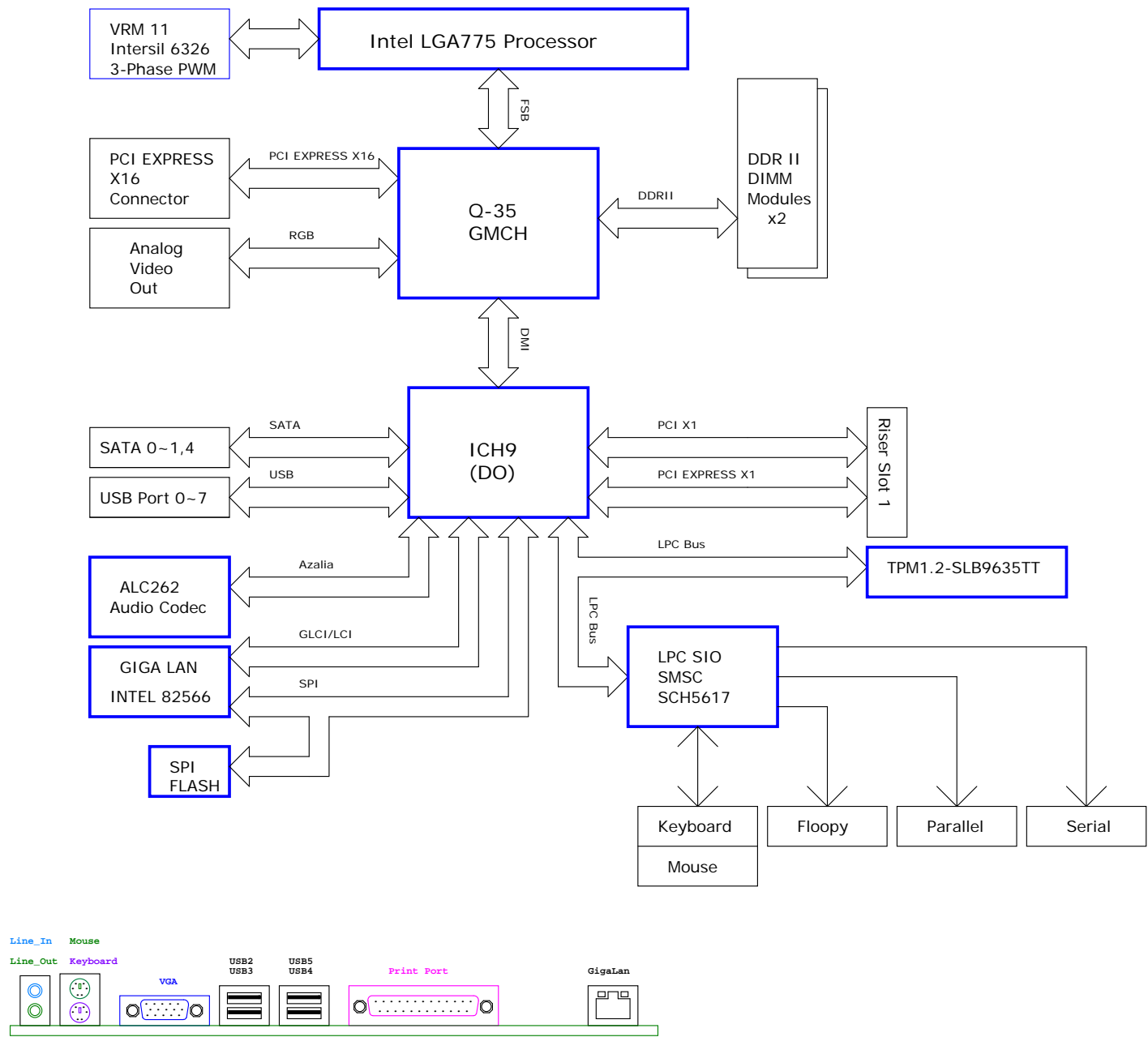
MS-6448 N1	ERP Number	Function
MS-7415-0B	601-7415-B10	Mainboard
MS-4046-2A	604-4046-020	Power Button/LED board
MS-4085-10	604-4085-020	Front Audio Board
MS-4048-3A	604-4048-040	Front 1394/USB Board
MS-4121-10	604-4121-010	Riser Card

Model option table

Model type	Function	BOM Config	ERP BOM No	BOM Opt.
MS-7415N1-0A	Bearlake Q35+ICH9 DO+Nineveh82566	Cfg-7415-L2B	601-7415-A10	L2B
MS-7415N1-0B	Bearlake Q35+ICH9 DO+Nineveh82566	Cfg-7415-L2B	601-7415-B10	L2B

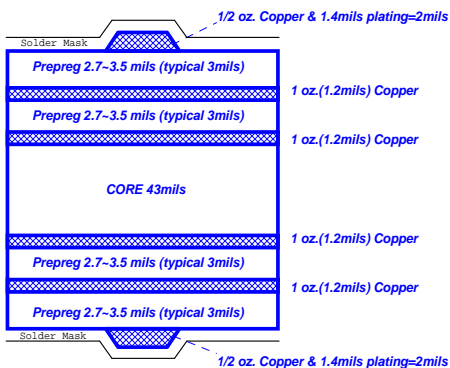
Cover Sheet	1
Block Diagram	2
Intel LGA775 CPU (P3:Signal,P4:Power,P5:GND)	3-5
CLOCK Generator-ICS9LP505-1	6
Bearlake Q35 - MCH	7-10
DDR II System Memory 1 & 2	11
DDR II VTT Decoupling & TPM1.2	12
PCI EXPRESS X16 Slot	13
Intel ICH9(DO) - PCI & DMI & USB & PCI-E	14
Intel ICH9(DO) - SPI&SATA&HOST&LPC&MISC	15
Intel ICH9(DO)- POWER&GND	16
RISER Slot & JCR & SATA Connector	17
LAN-NINEVEH 82566	18
FAN Control/Detect	19
HD AUDIO-ALC262 & Front Panel	20
SIO SMSC SCH5617 & FDD	21
KB/MS/LPT/COM Port /FAN	22
VGA Connector	23
USB Connectors	24
ATX Connetcor & IR	25
ACPI CONTROLLER MS7	26
DIMM/GMCH/AMT POWER	27
VRM11 Intersil 6326 3Phase	28
Manual parts	29
GPIO & Jumper Setting	30
Power MAP	31
History	32

Block Diagram



Board Stack-up (6 layers)

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
Differential Clock : 18/4/10/4/18

Example Fab Drawing Note (1080 Prepreg PCB)


Trace Width (mils)	Differential Spacing (mils)	Target Impedance	Tolerance
4.0	NA	50-ohm, single-ended	15%
6.5	NA	40-ohm, single-ended	15%
7.5	NA	37-ohm, single-ended	15%
9.5	NA	32-ohm, single-ended	15%
3.9	8.1	95-ohm, differential	20% reference only
4.5	7.5	90-ohm, differential	20% reference only

Bearlake(GMCH) Impedance Requirements by Interface

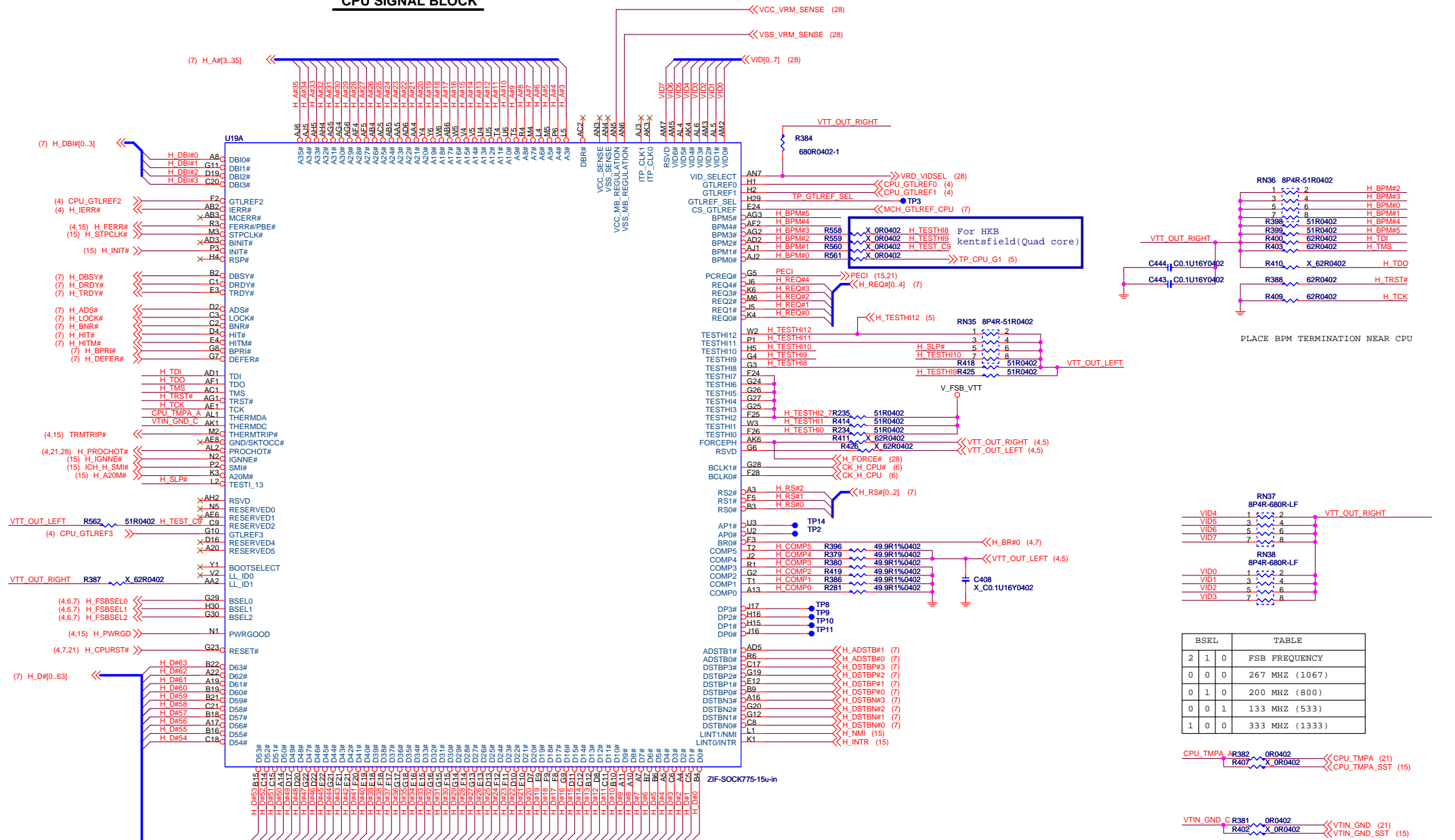
Interface	Impedance Required
FSB(All)	4x signals 42-ohm, others 50-ohm, single-ended
Controller Link	50-ohm, single-ended
DDR2(DQ, DQS, DM, CLK, CLK#)	40-ohm, single-ended
DDR2(Control)	43-ohm, single-ended
DDR2(Command)	33-ohm, single-ended
DDR3(CLK, CLK#)	36-ohm, single-ended
DDR3(DQ, DQS, DM)	50/37-ohm, single-ended
DDR3(Control)	36-ohm, single-ended
DDR3(Command)	32-ohm, single-ended
PCI Express, DMI	95-ohm, differential
VGA	87-ohm, single-ended at MCH breakout, then 50-ohm, single-ended to VGA connector

ICH9 Impedance Requirements by Interface

Interface	Impedance Required
PCI	50-ohm, single-ended
Controller Link	50-ohm, single-ended
Miscellaneous	50-ohm, single-ended
PCI Express, DMI	95-ohm, differential
SATA	95-ohm, differential
USB	90-ohm, differential

 MICRO-START INTL CO., LTD.		
Title BLOCK DIAGRAM		
Size	Document Number MS-7415	Rev 0B
Date:	Thursday, December 20, 2007	Sheet 2 of 32

CPU SIGNAL BLOCK




BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)
1	0	0	333 MHZ (1333)

CPU_TMPA_AR382 0R0402
R407 X_0R0402

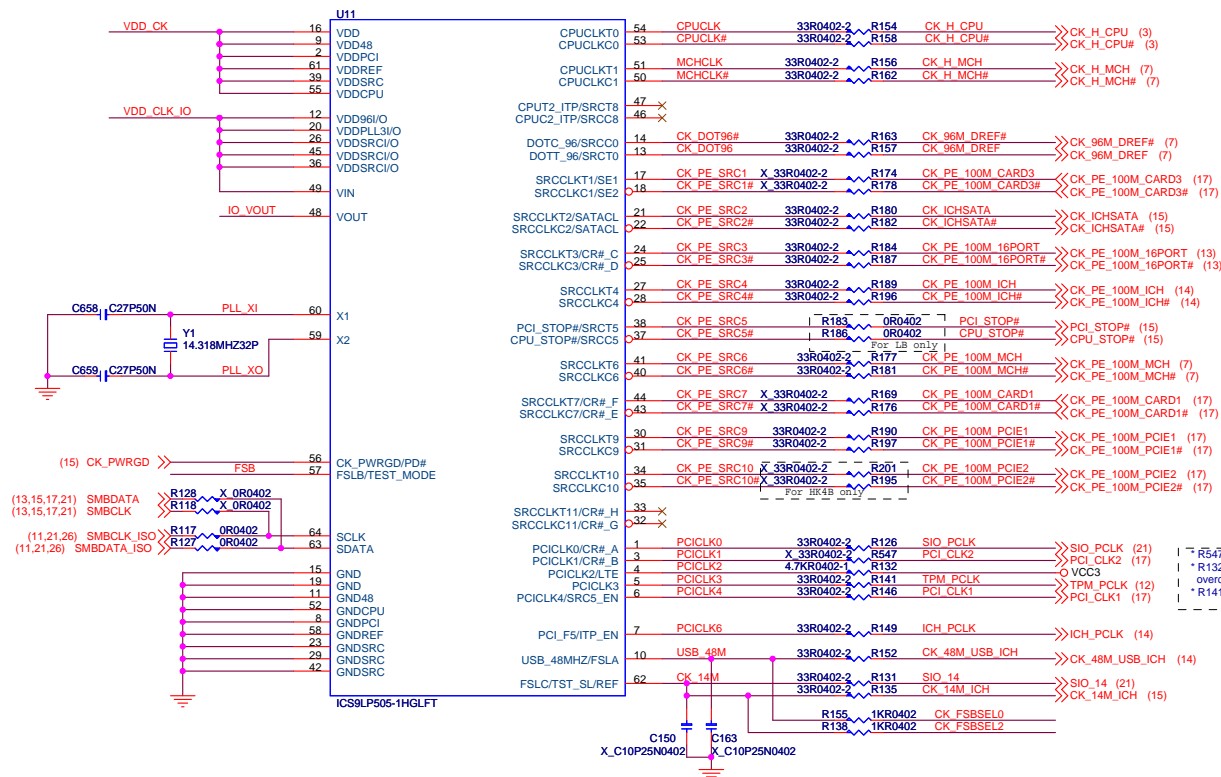
CPU_TMPA (21)
CPU_TMPA_SST (15)

VTIN_GND C R381 0R0402
R402 X 0R0402

VTIN_GND (21)
VTIN_GND_SST (15)

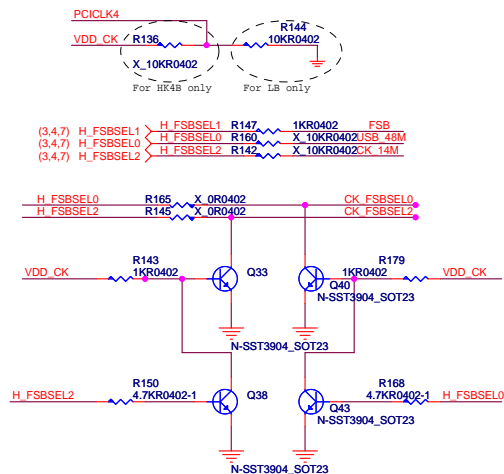
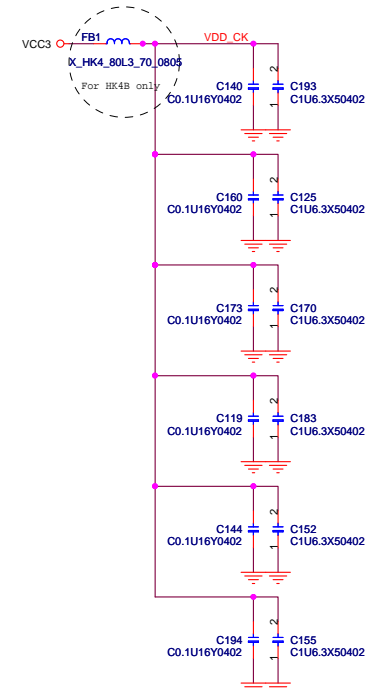
 MSI <i>Link to the Future</i>				MICRO-START INT'L CO.,LTD.			
Title							
INTEL LGA775 GND							
Size	Document Number					Rev	
	MS-7415					0B	
Date:	Thursday, December 20, 2007			Sheet	5	of	32

CLOCK Generator - ICS9LP505-1HGLFT



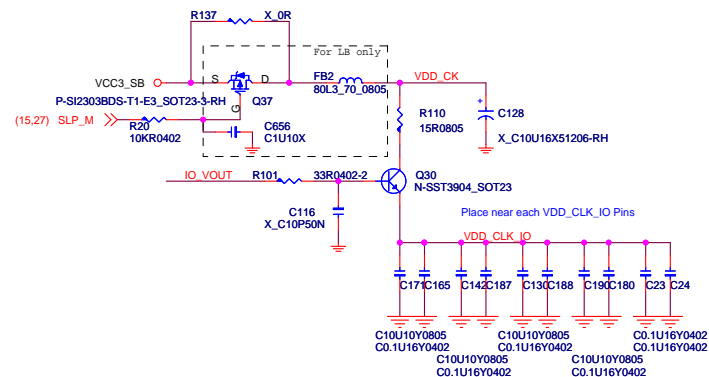
VDD_CK Decoupling

Place near each VDD_CK Pins

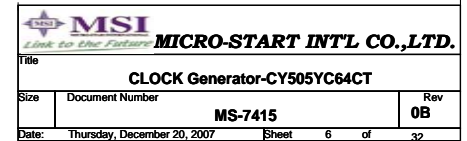
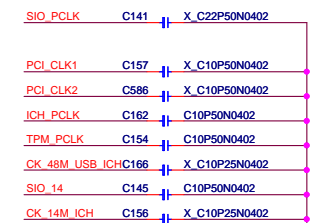


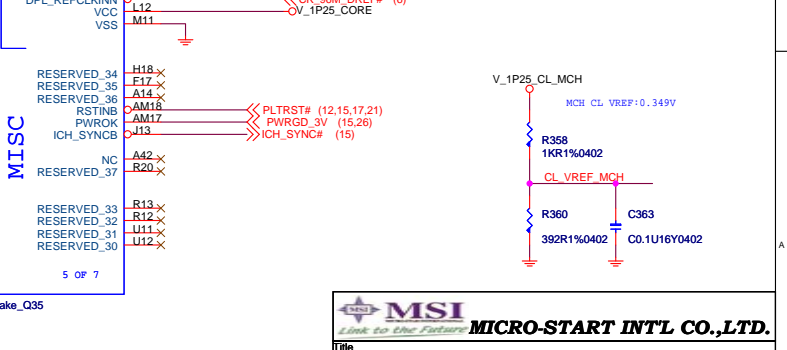
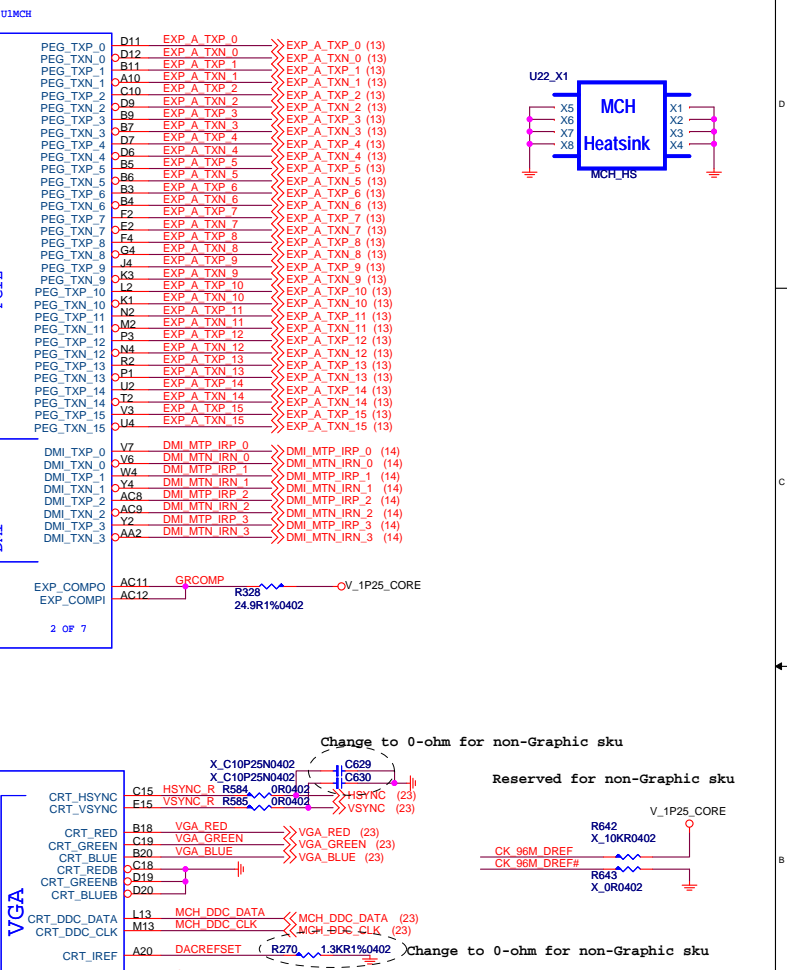
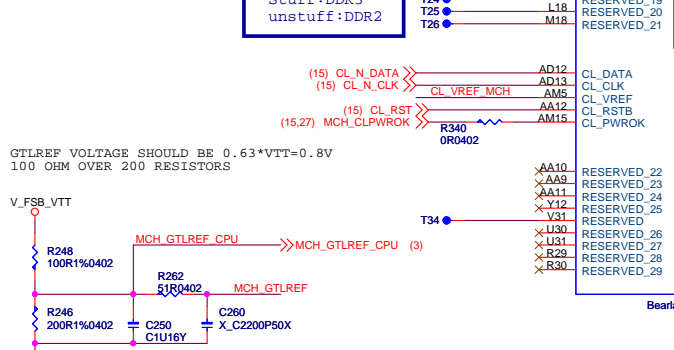
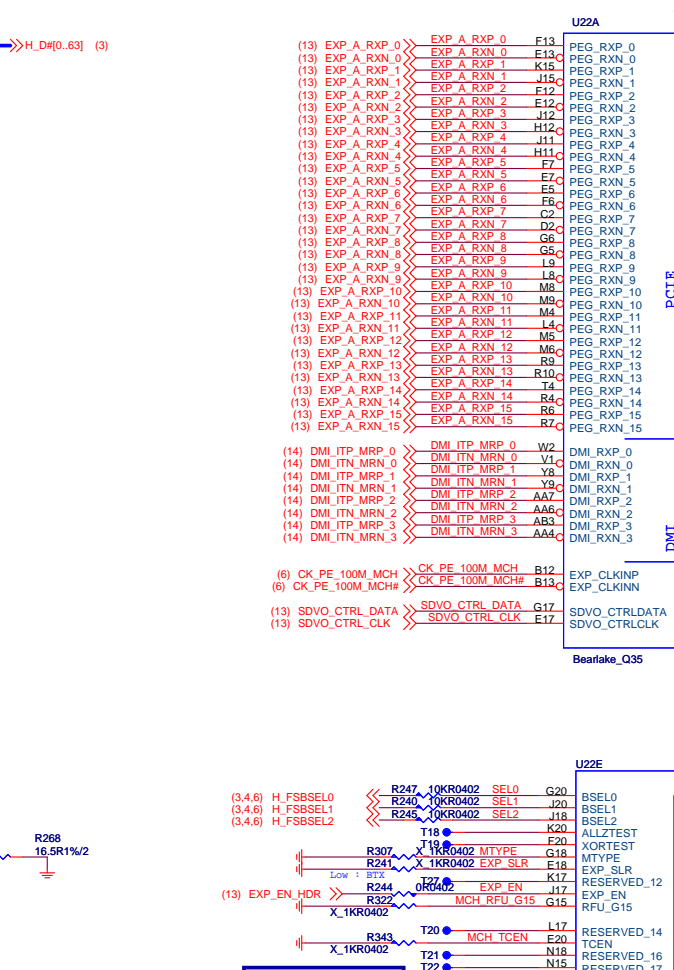
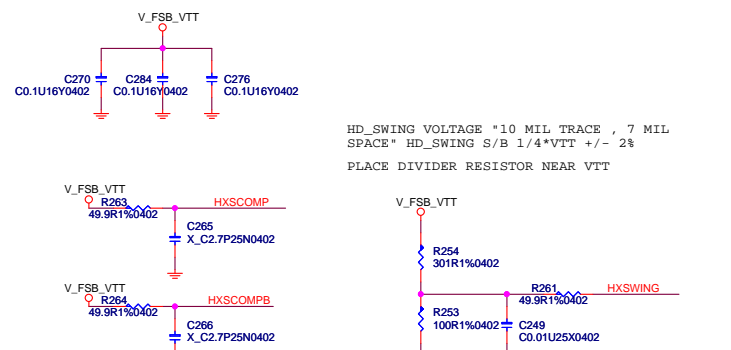
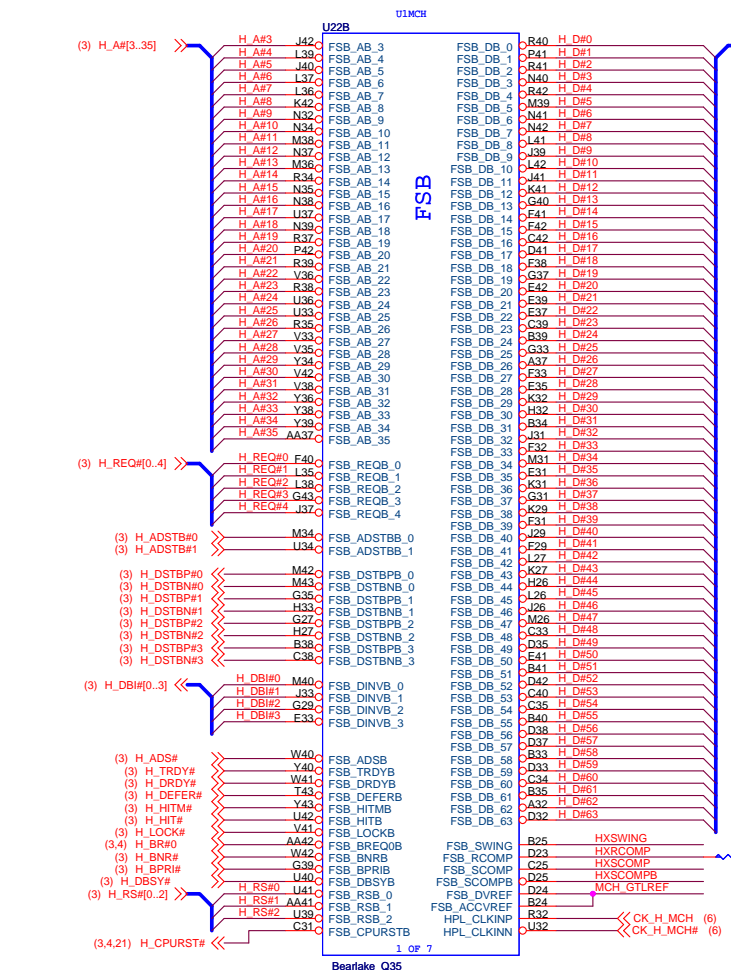
FSC Bit7	FSB Bit6	FSA Bit5	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00

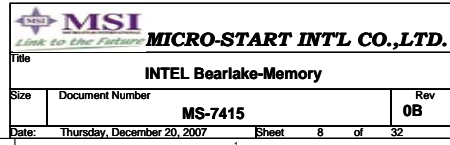
VDD_CK & VDD_CLK_IO Power

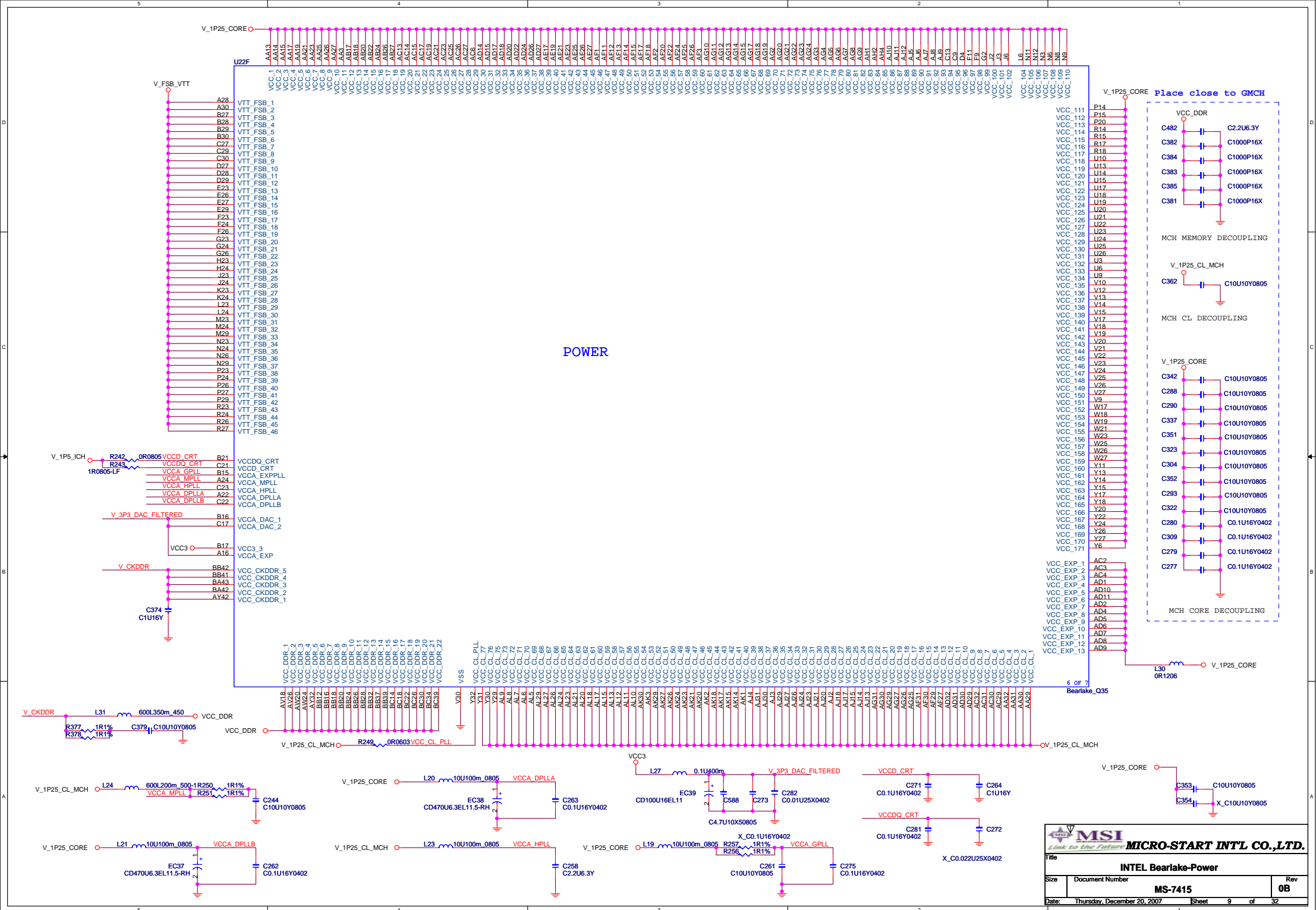


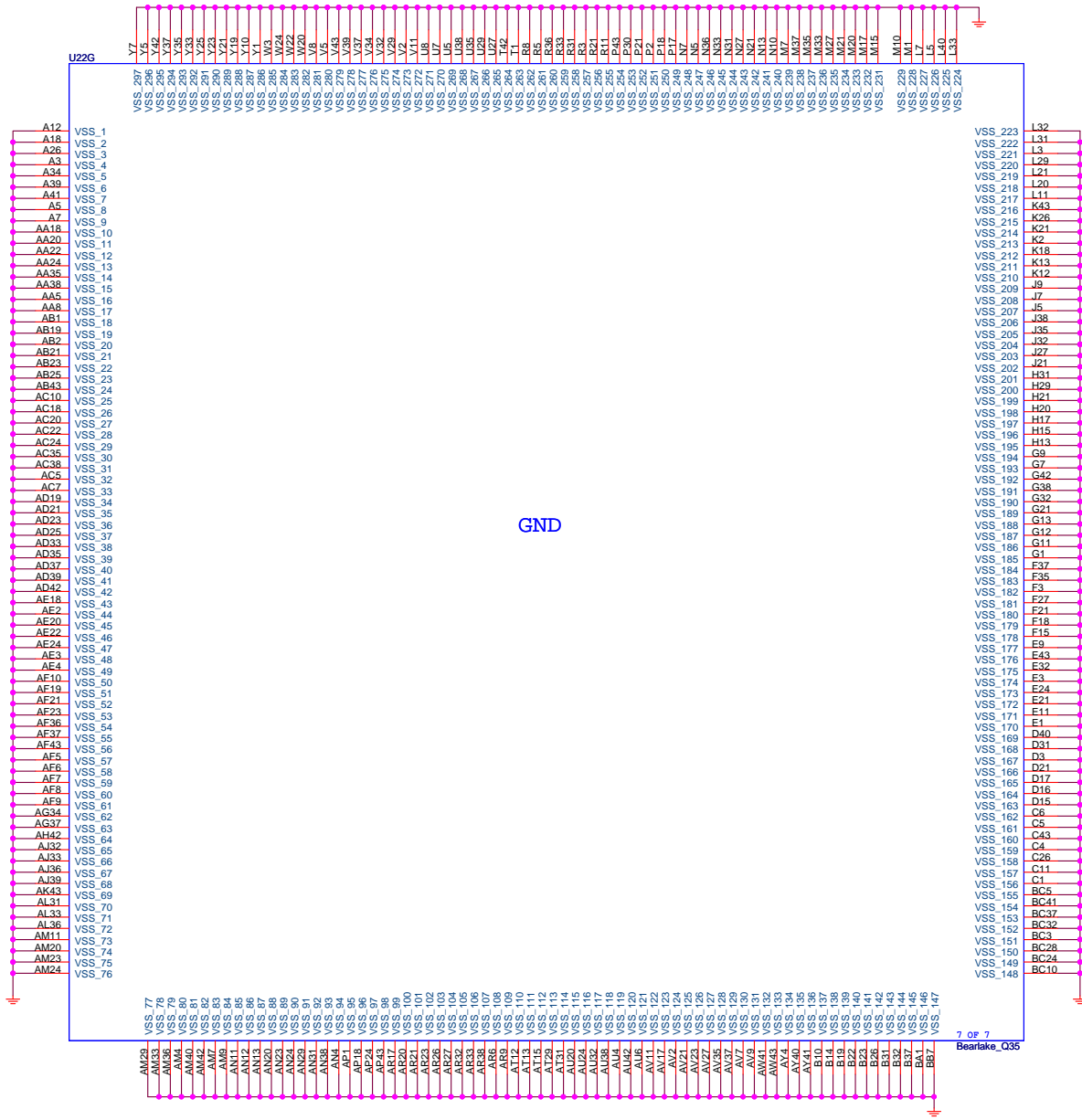
For EMI reserver

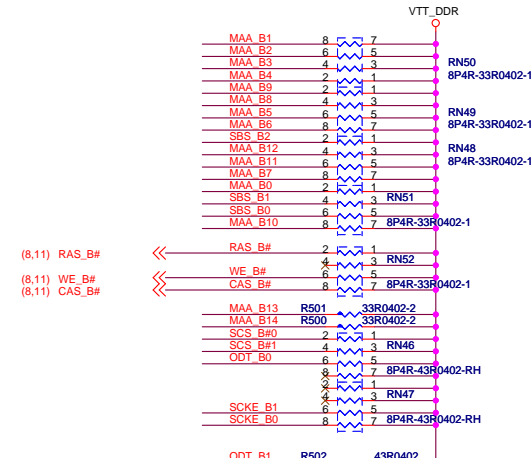
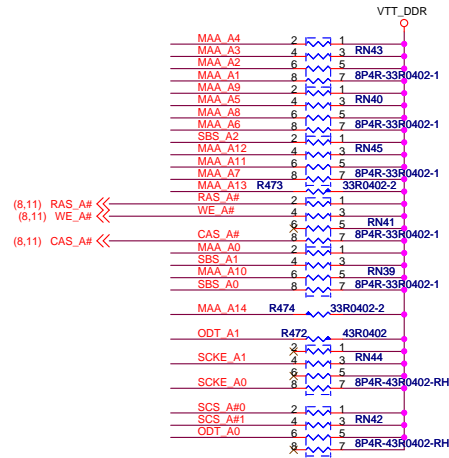
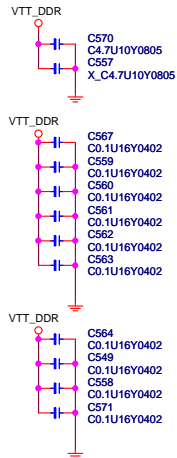
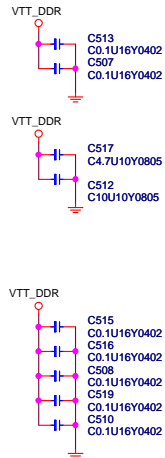




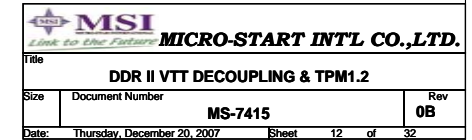
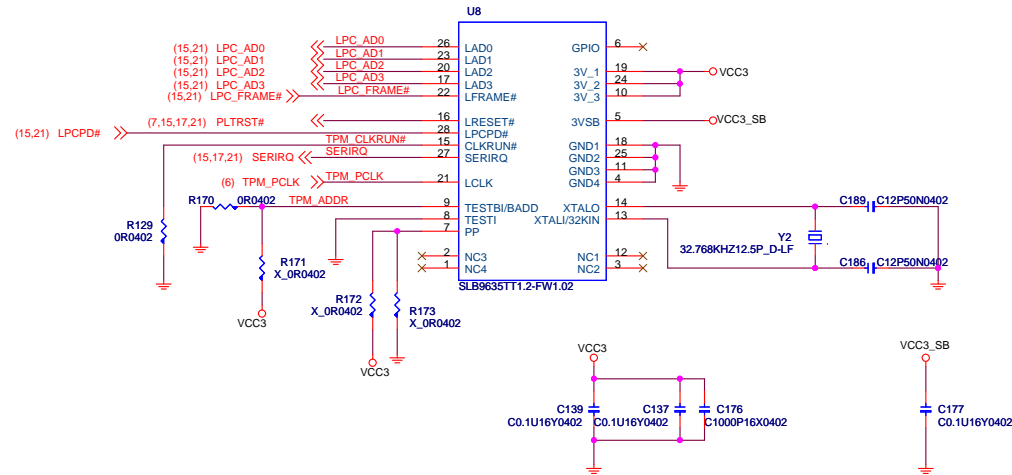
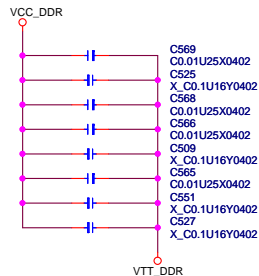
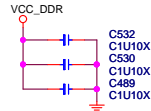
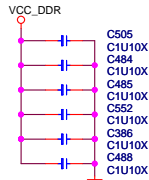
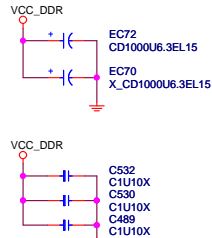




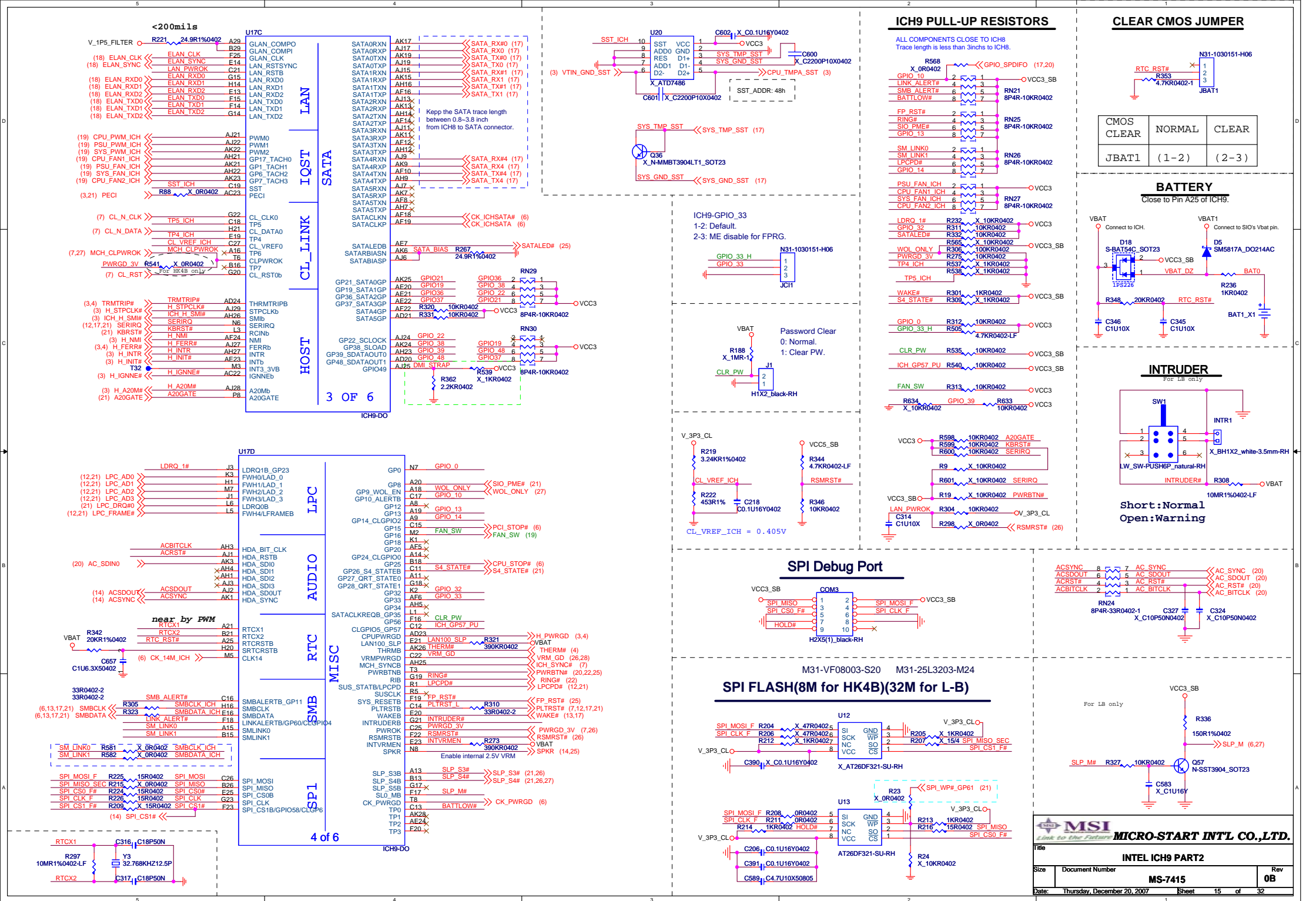


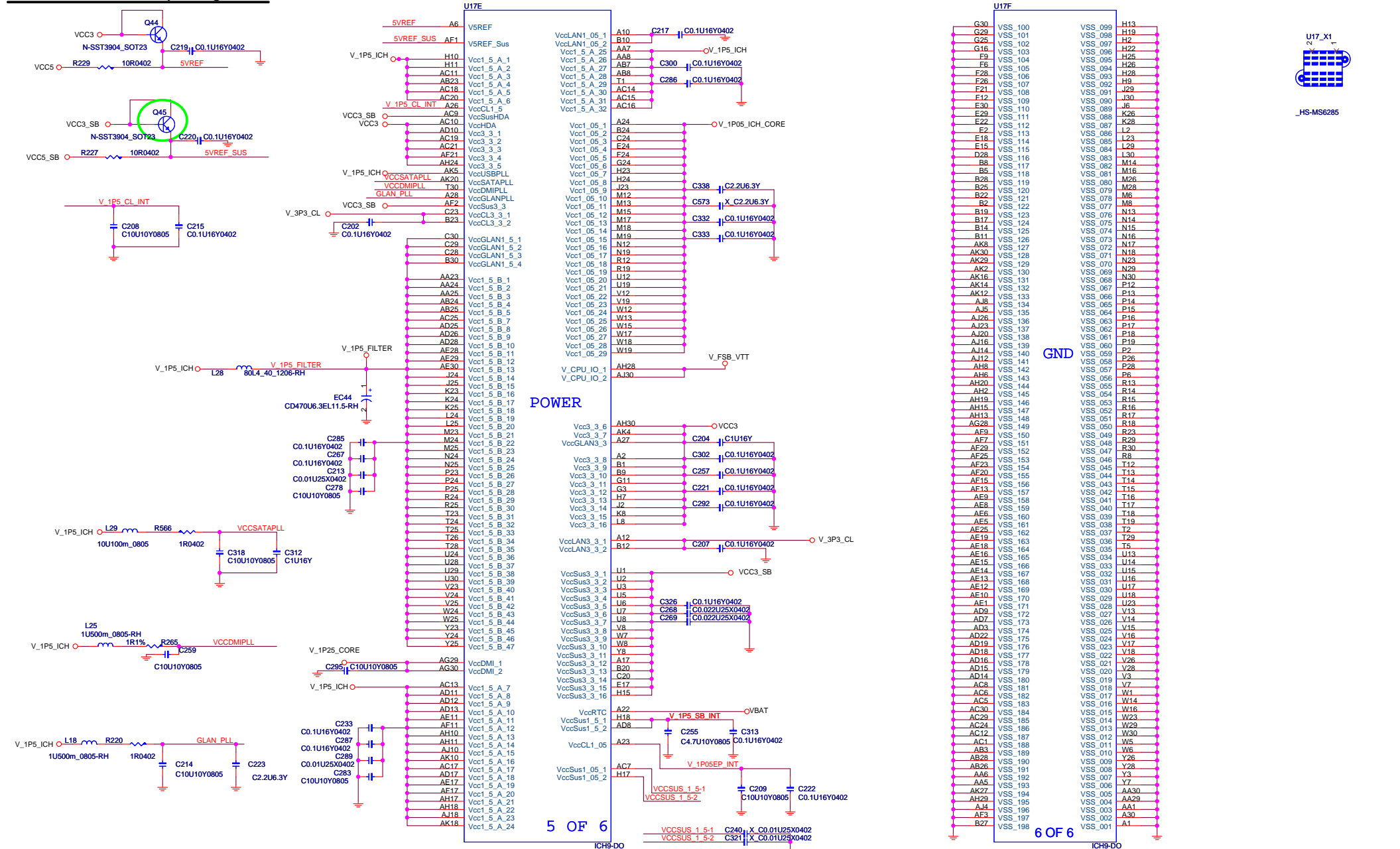


IO Address: 0x02E

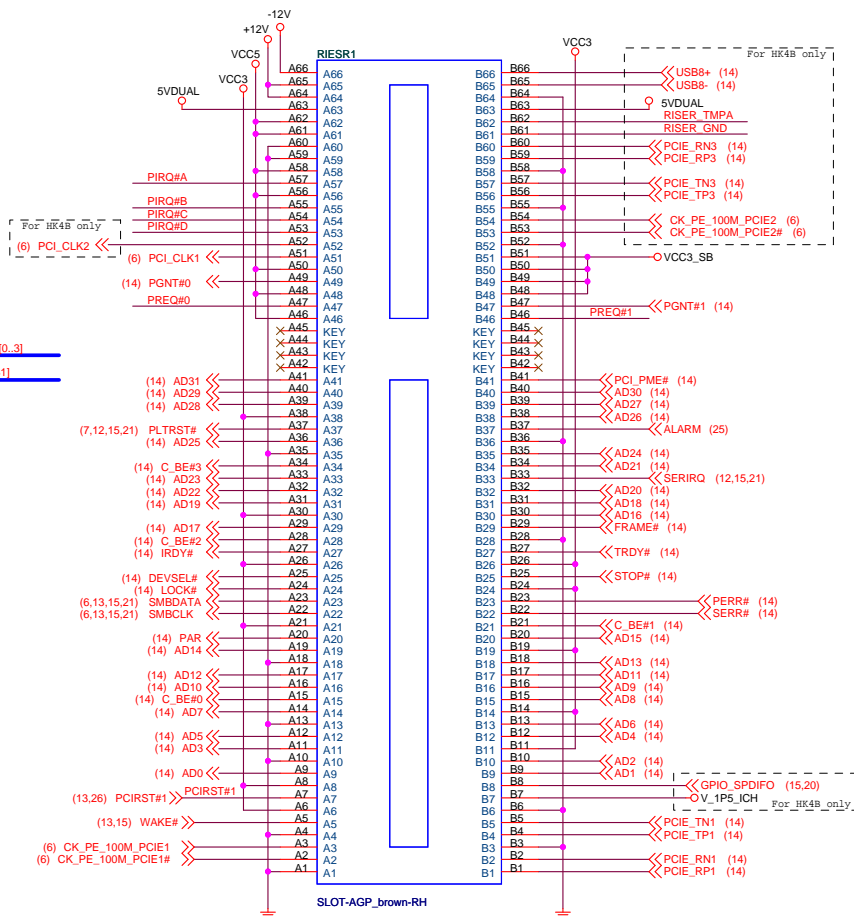








LB&HK4B riser card interface

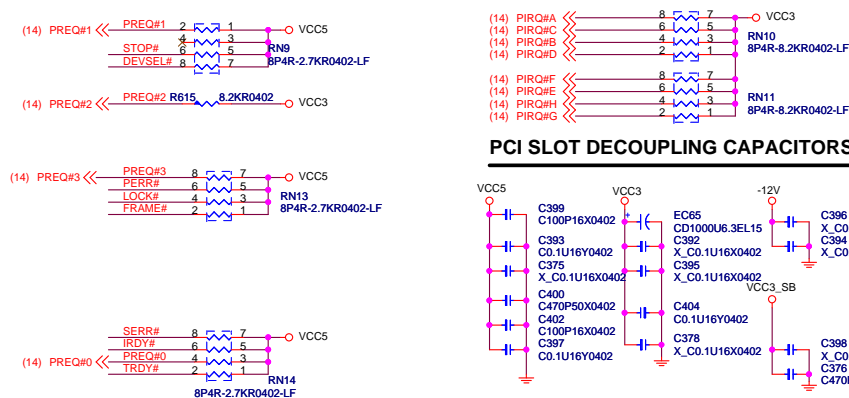


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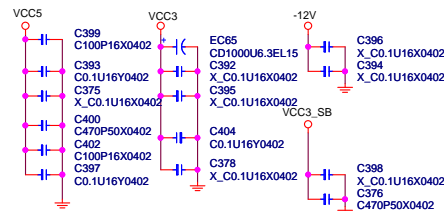
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

```

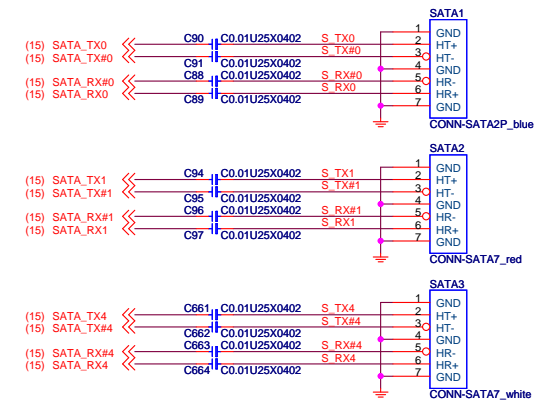
PCI PULL-UP / DOWN RESISTORS



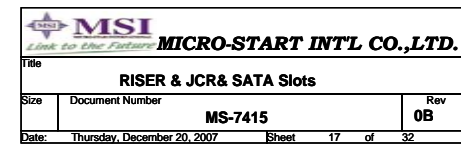
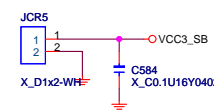
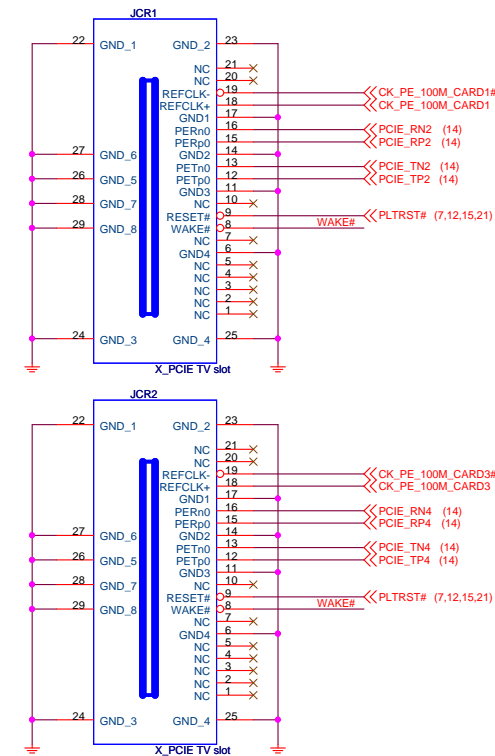
PCI SLOT DECOUPLING CAPACITORS



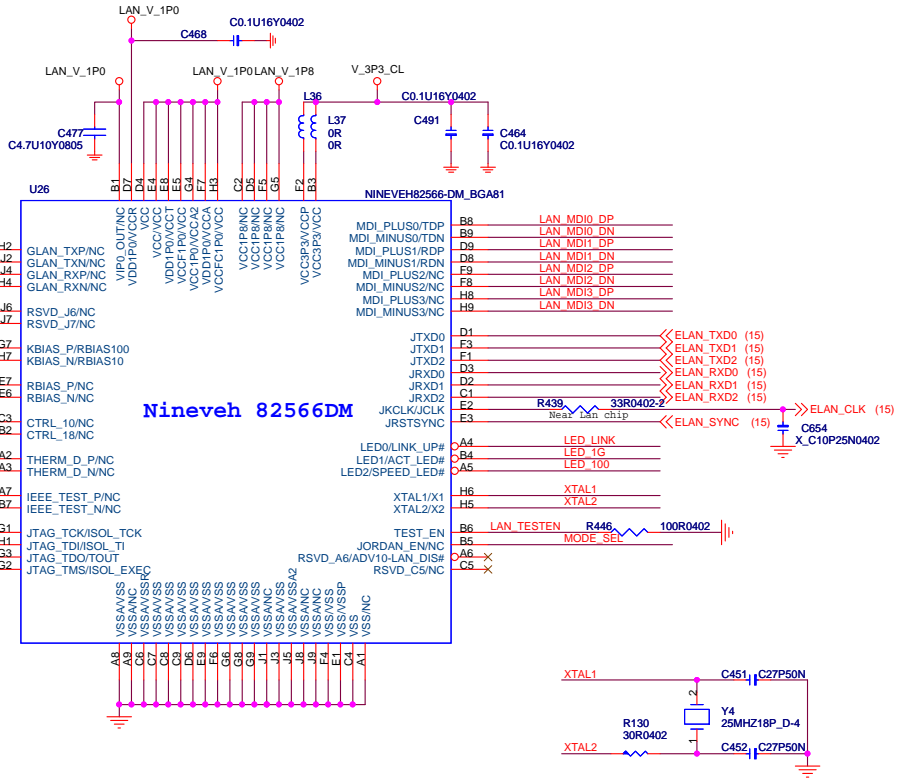
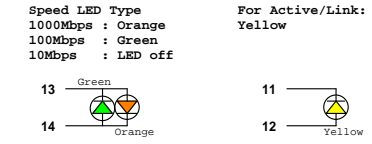
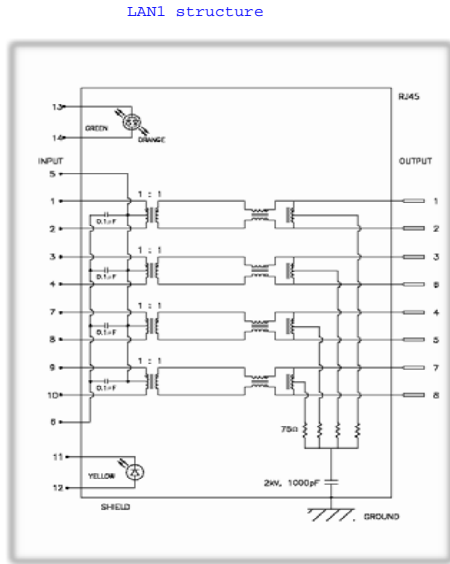
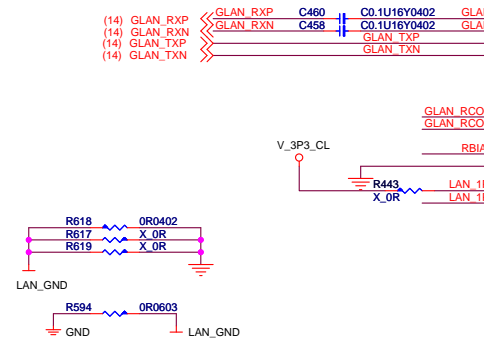
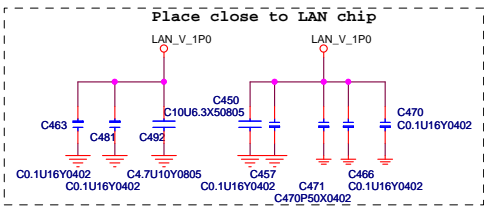
SERIAL ATA CONNECTOR BLOCK



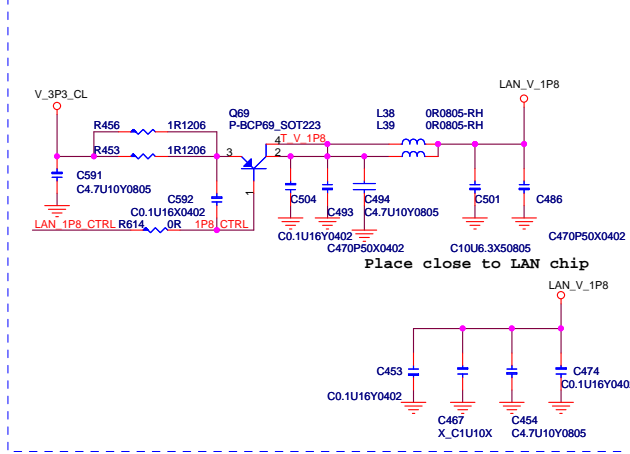
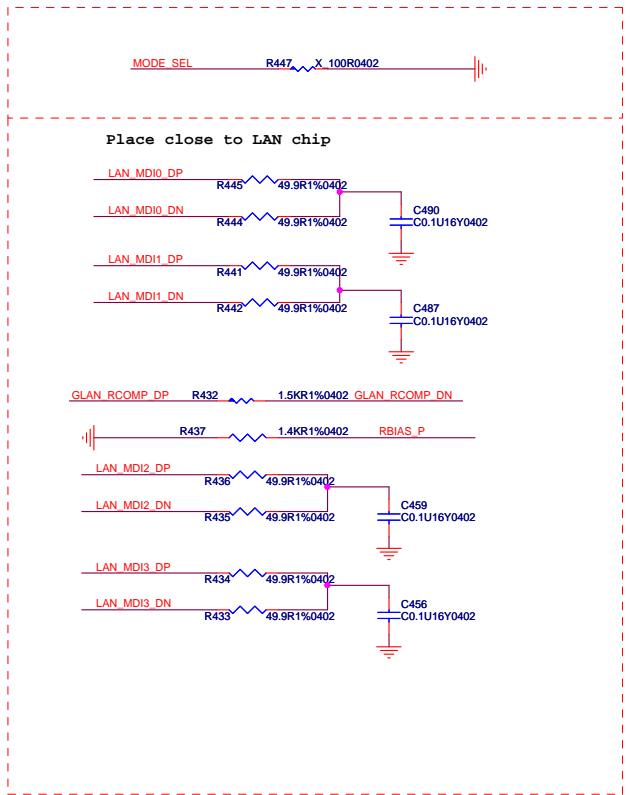
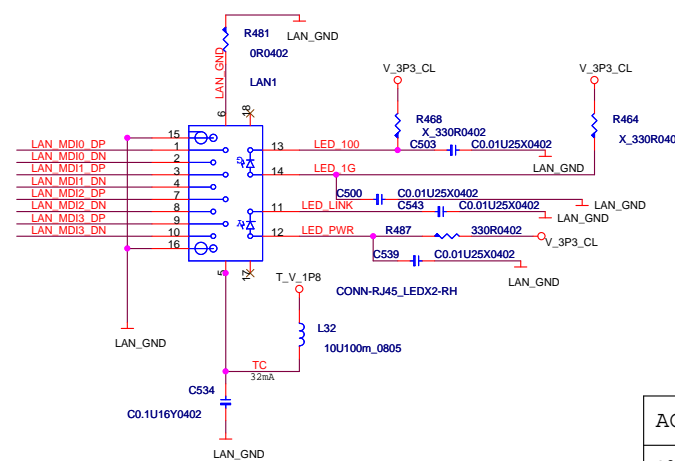
```
Lunar Bear not mount : JCR1, JCR2 & JCR5
HK4B : populate JCR1, reserve JCR2 & JCR5
```



LAN - NINEVEH



LAN CONNECTOR



ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW
	WOL DIS-->HIGH

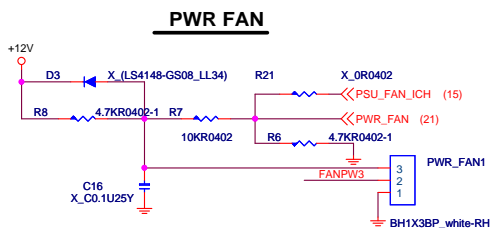
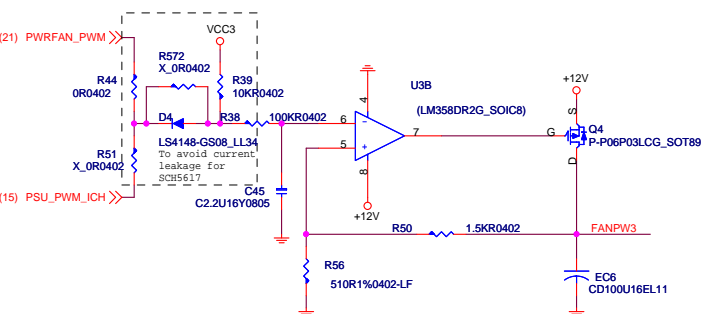
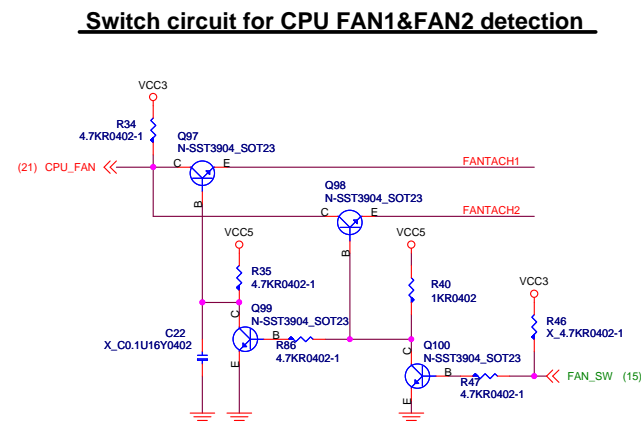
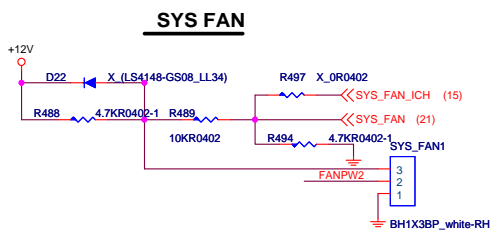
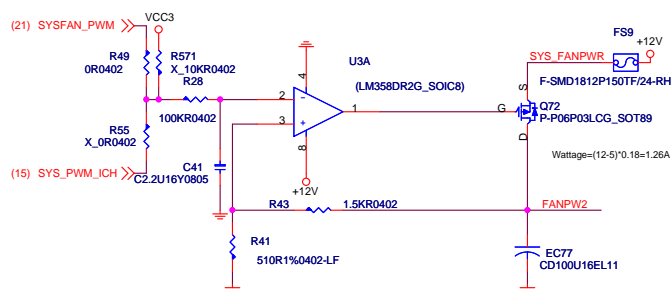
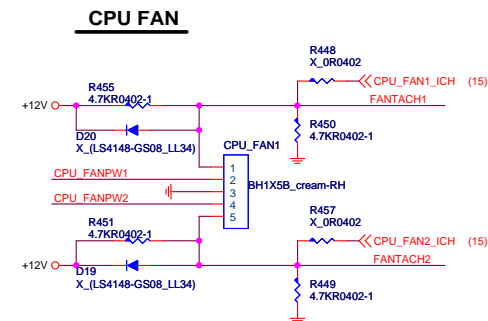
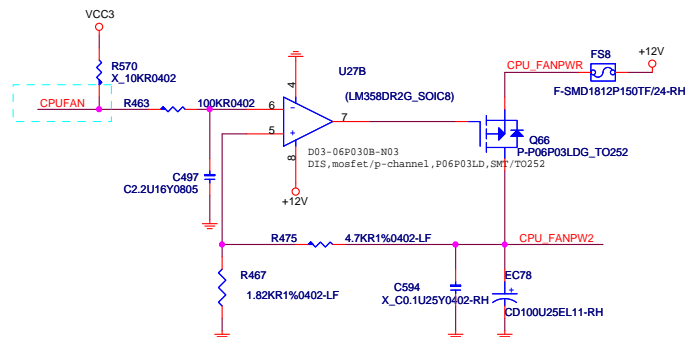
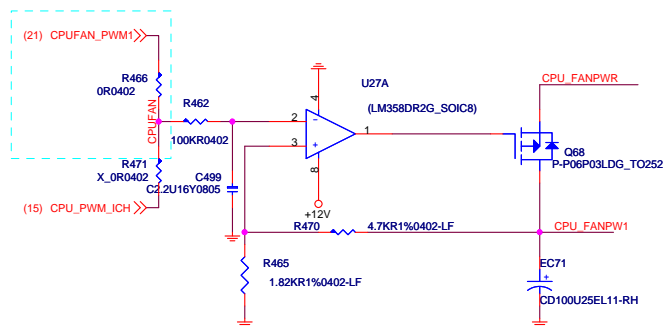
MSI
Link to the Future

MICRO-START INT'L CO.,LTD.

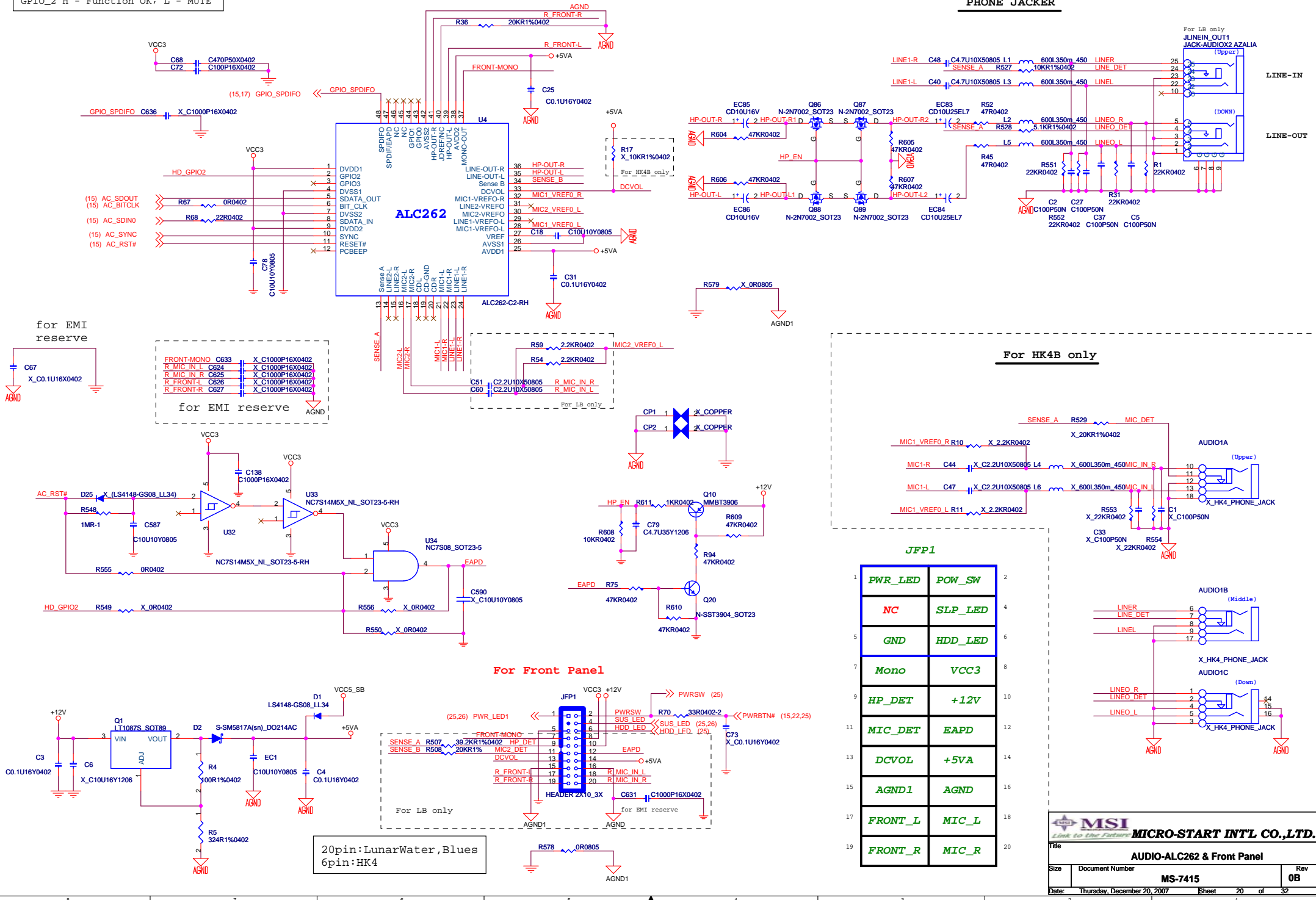
Title: **LAN-NINEVEH 82566**

Size: Document Number: **MS-7415** Rev: **0B**

Date: Thursday, December 20, 2007 Sheet 18 of 32



GPIO_2 H - Function OK; L - MUTE



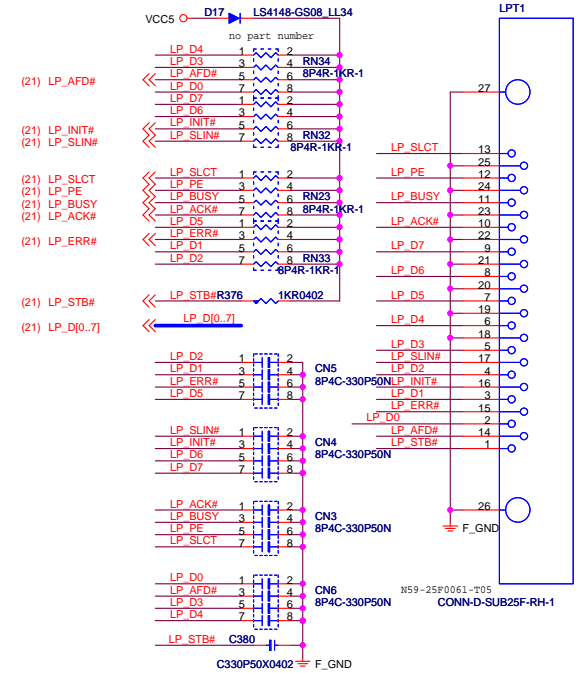
For LB only



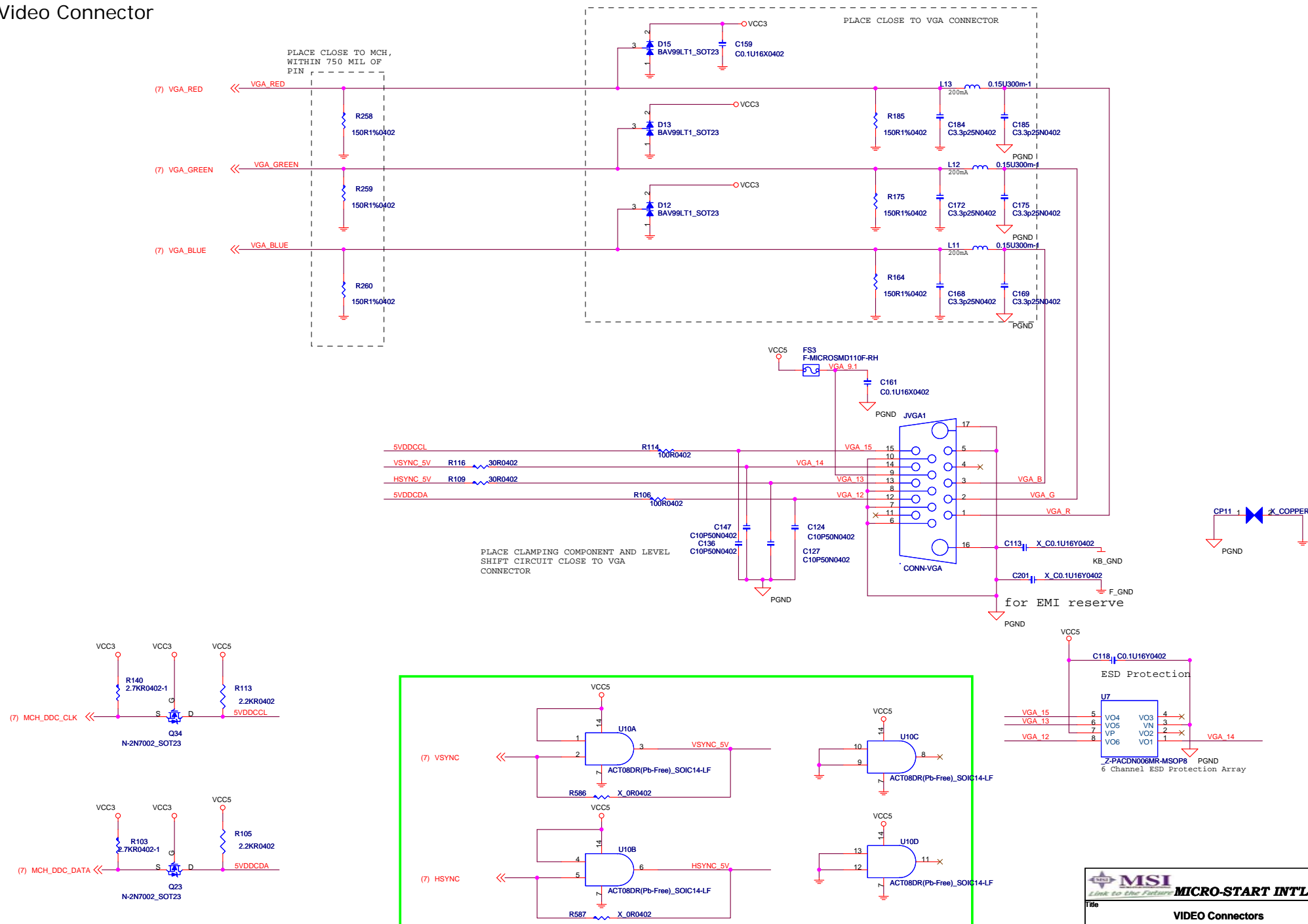
PS2 KEYBOARD & MOUSE CONNECTOR

	LB	HK4B
FS1	Yes	No
FS2	No	Yes
R93	Yes	No
R60	No	Yes
R64	No	Yes
L8	Yes	No
L10	Yes	No
C76	Yes	No
C101	Yes	No

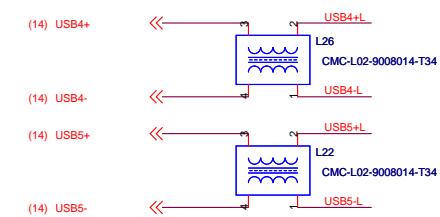
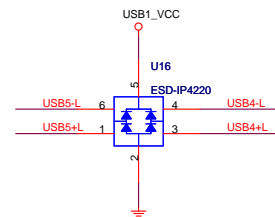
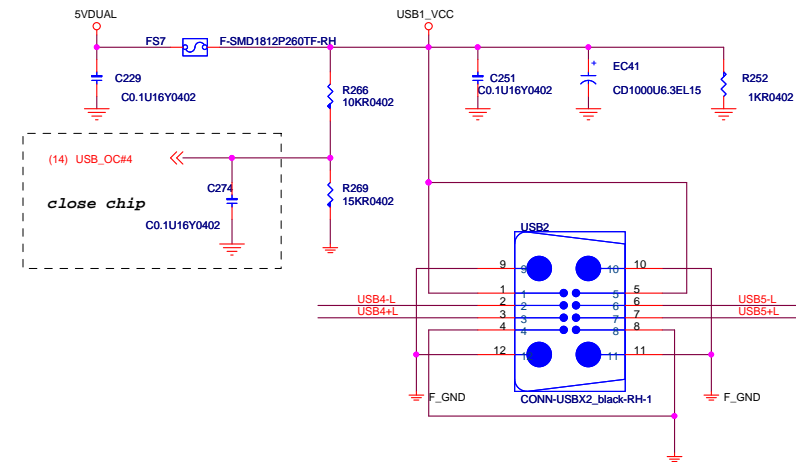
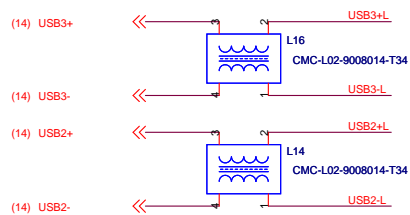
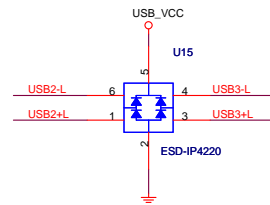
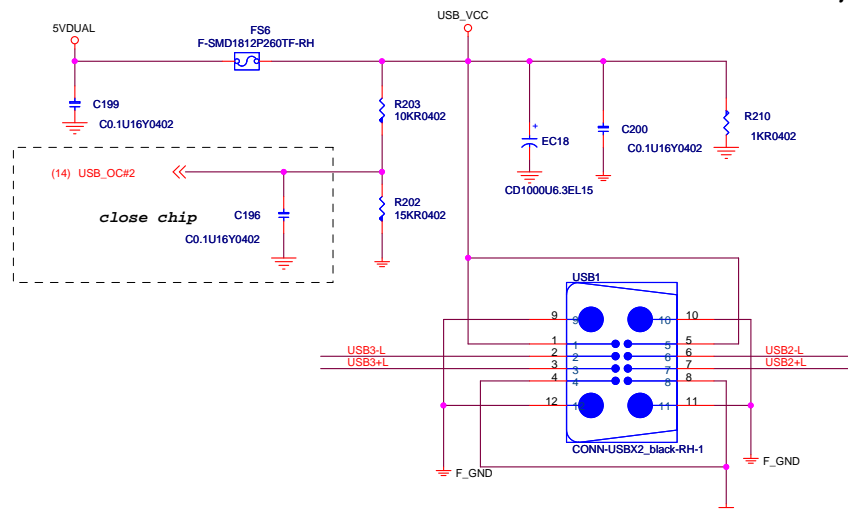
For LB only



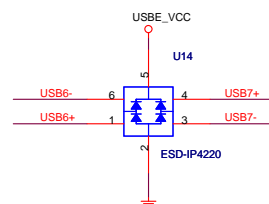
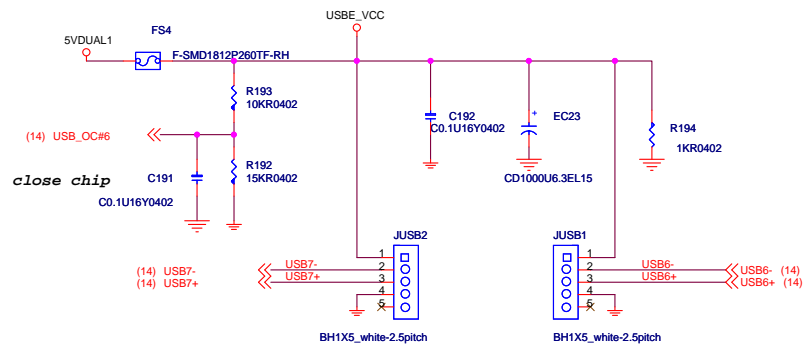
Video Connector



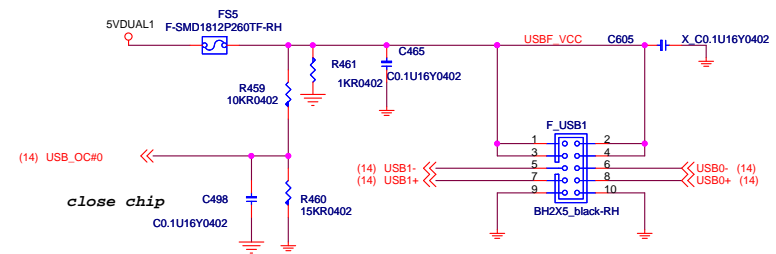
REAR USB PORT



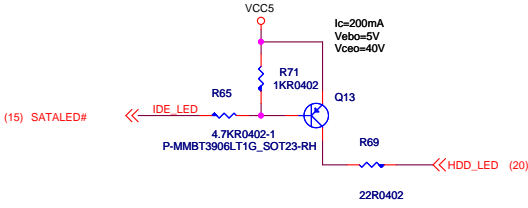
EXTERNAL USB PORT 0,1



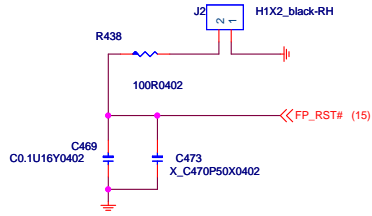
FRONT PANEL USB PORT 6,7 CONNECTOR



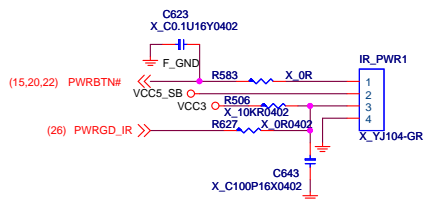
ATX connector / IR



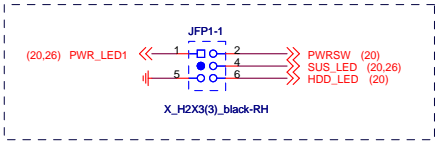
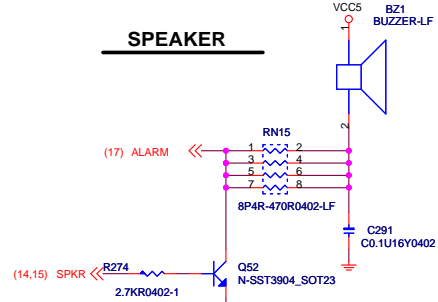
For Debug
Remove after MP



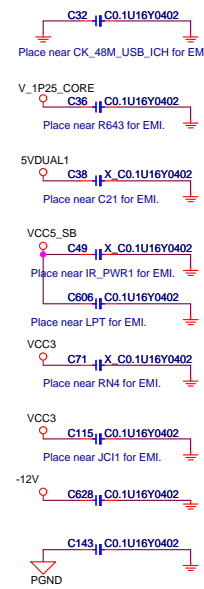
IR Connector



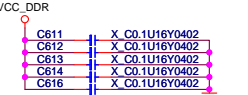
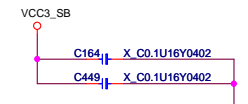
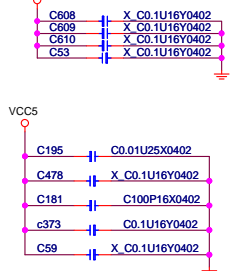
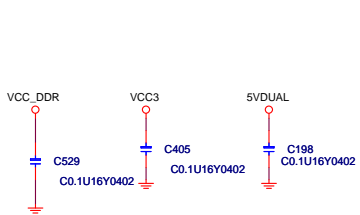
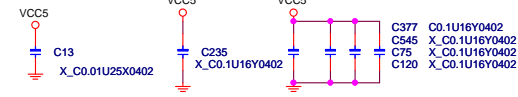
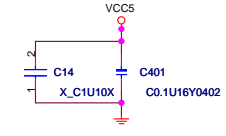
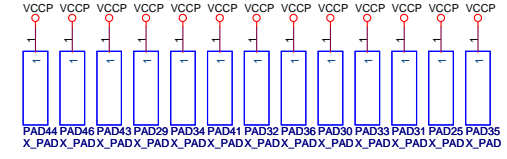
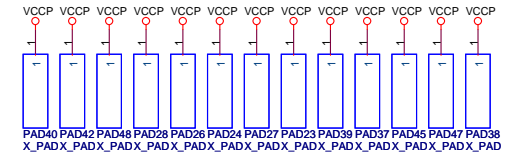
SPEAKER



EMI CAPs for L2B

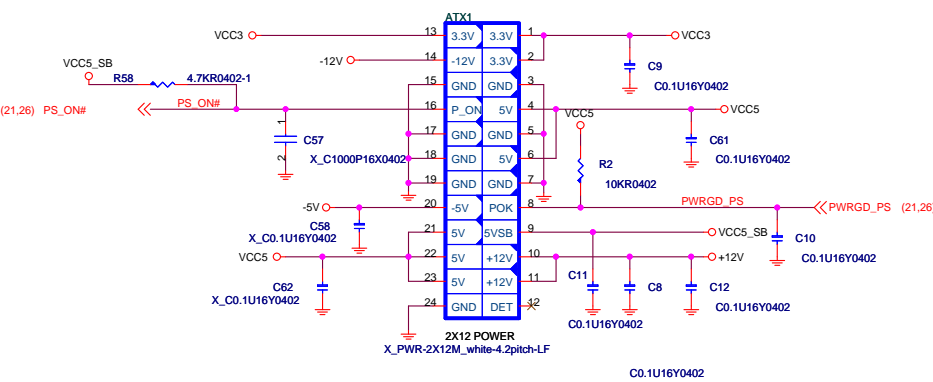


for EMI reserve

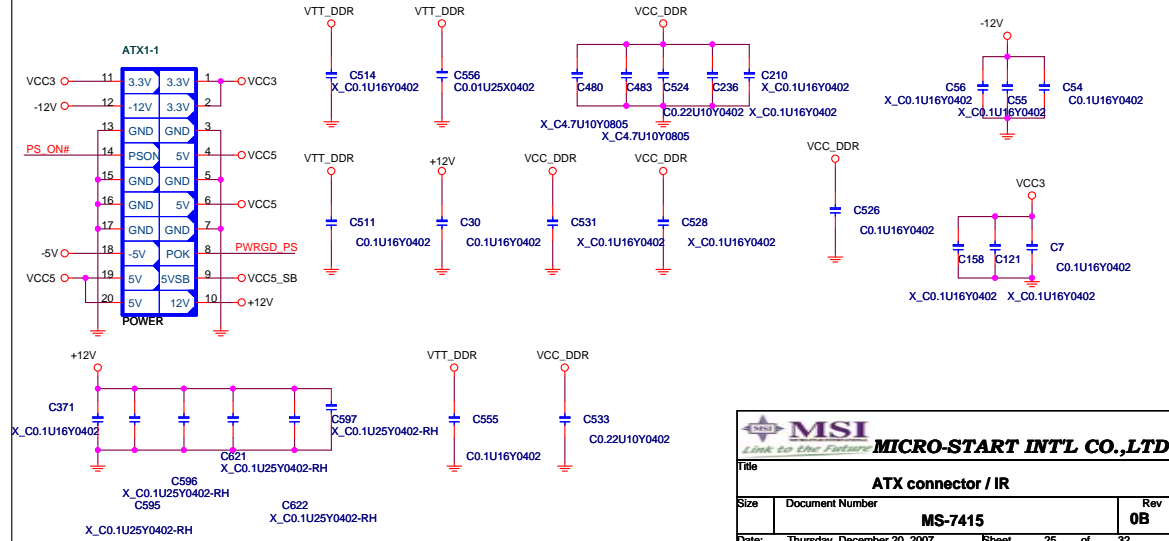


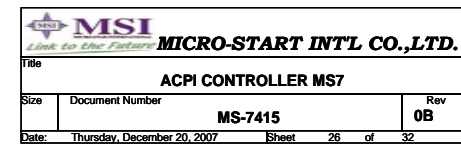
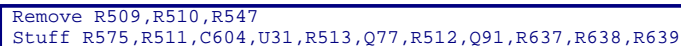
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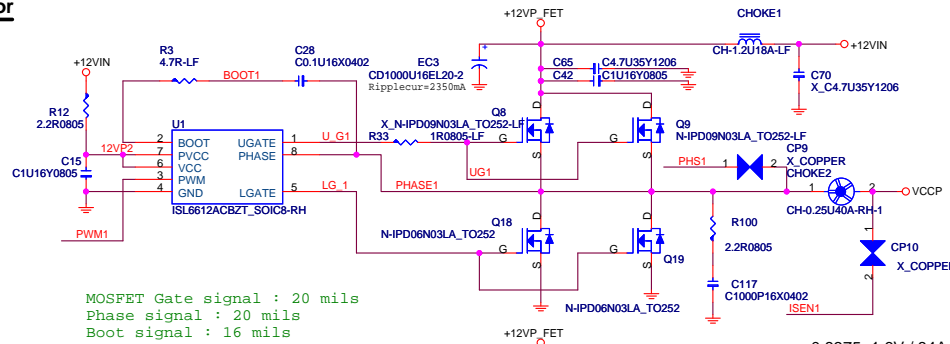
ATX Connector



11,12,23,24pin:reserve







EL Capacitors

VCCP

EC9
CD1800U6.3EL20-3

EC10
CD1800U6.3EL20-3

EC12
CD1800U6.3EL20-3

VCCP

EC7 1+ 2 X CD820U2.5FP-1

EC8 1+ 2 CD820U2.5FP-1

EC11 1+ 2 CD820U2.5FP-1

EC13 1+ 2 CD820U2.5FP-1

EC14 1+ 2 CD820U2.5FP-1

EC15 1+ 2 CD820U2.5FP-1

EC16 1+ 2 CD820U2.5FP-1

EC17 1+ 2 CD820U2.5FP-1

The diagram illustrates the connection of three HS-MS7033 modules (HS1, HS3, HS2) to a common ground. Each module has a ground pin connected to a common ground line.

VCCP

C644 X_C100P16X0402

C646 X_C100P16X0402

C648 X_C100P16X0402

C650 X_C100P16X0402

C652 X_C100P16X0402

+12VP_FET

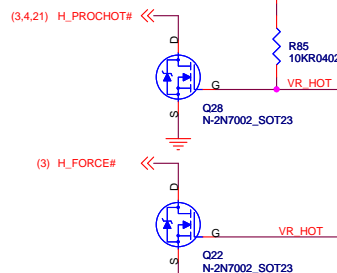
C645 X_C100P16X0402

C647 X_C100P16X0402

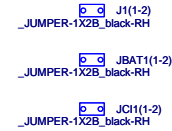
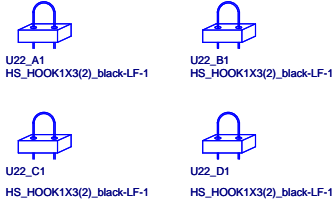
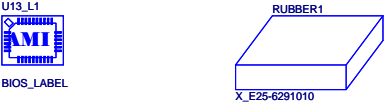
C649 X_C100P16X0402

C651 X_C100P16X0402

Remove Q8/Q14/Q16 for 65W CPU.



Auto-BOM Manual Parts



JFP1

1	PWR_LED	POW_SW	2
	NC	SLP_LED	4
5	GND	HDD_LED	6

For HK4B

ICH9

GPIO Pin	Type	Default	Function	Power	MUXED / UNMUXED	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK21
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE/GPIO9, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPI	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	NC	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPI	Pull-up VCC3_SB with 10K	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# for CK505(Not Use)	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	FAN switch, pull_up VCC3 with 10K.	VCC3	UNMUXED	M2
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	NC	VCC3	UNMUXED	K1
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	NC	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K(Not Use)	VCC3	MUXED	J3
GPIO 24	I/O	GPO	NC	3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# for CK505(Not Use)	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE#	3.3V_SB		C11
GPIO 27	I/O	GPO	NC	3.3V_SB		A11
GPIO 28	I/O	GPO	NC	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#4 connect to USB connector	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#6 connect to USB connector	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#6 connect to USB connector	3.3V_SB		M1
GPIO 32	I/O	GPO	Pull up VCC3 with 10k	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	Pull-up to VCC3 with 4.7K through JC11 Jumper.(Default)	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	NC	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	NC	VCC3		L1
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPI	Pull-down to GND with 10K directly	VCC3		AH23
GPIO 40	I/O	OC1#	OC#0 connect to USB connector	3.3V_SB		N3
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	3.3V_SB		P7
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	3.3V_SB		R7
GPIO 43	I/O	OC4#	OC#4 connect to USB connector	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#6 connect to USB connector	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#6 connect to USB connector	3.3V_SB		T7/P1
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping ,pull-down 2.2K to GND	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#	VCC3	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3#(Not Use)	VCC3	MUXED	F7
GPIO 56	I/O	GPI	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPI	Pull-up to VCC3_SB with 10K directly	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS#(Not Use) , SPI_CS1_F#(Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	LINKALERT# pull-up to VCC3_SB with 10K	3.3V_SB		F18

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Riser slot (PCI1)	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1
Riser slot (CARD1)	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#0 PGNT#0	AD18	PCI_CLK2

DDR2 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A1/SCLK_A1# SCLK_A2/SCLK_A2#
DIMM 2	0A4H	SCLK_B0/SCLK_B0# SCLK_B1/SCLK_B1# SCLK_B2/SCLK_B2#

SIO - SMSC-5617 Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP76	53	GPIO_KB	OUTPUT
GP41	77	SIO_PME#	OUTPUT

SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	SIO, ICH9, PCI EXPRESS[X16][X1]
SMBCLK_ISO	VCC3	DIMM, CLK GEN, MS7

Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
JC11	(1-2)Normal	(2-3)ME Disable for FPROG
J1	(1-2)short: Normal	(1-2)Open: Clear PW

LGA775-CPU		
0.8375V - 1.6000V Core	-	100A
1.2V FSB Vtt	-	4.6A

Bearlake (GMCH)		
1.2V FSB_VTT	-	1.2 A
1.25V Core	-	13.8A
1.25V DMI/PCI Exp.	-	2.47 A
1.8V VCC_DDR	-	3.73A
1.8V VCC_SMCLK	-	450mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.25V Vcc CL	-	4.3A

ICH9		
1.05V Core	-	1.16A
1.25V DMI	-	41 mA
1.2V FSB_VTT	-	2 mA
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

CK505		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

Nineveh GbE		
3.3V_SB I/O & LED	-	15.5mA
1.8V AVDD	-	418.2mA
1.0V Core	-	277.2mA

ISL6326		
VCCP VRD11/10.x	-	0.8375V-1.6000V
3-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.9V Linear 1.2A

MS11+ SW-Power		
VCC_DDR	-	1.8V PWM 18.43A

MS11+ SW-Power		
V_1P25_CORE	-	1.25V PWM 21.11A

MS7 Controller		
V_1P25_CL	-	1.25V Linear 4.3A
V_1P05_ICH	-	1.05V Linear 1.16A
V_FSB_VTT	-	1.2V Linear 5.8A
V_1P5_ICH	-	1.5V Linear 4.05A
VCC3_SB	-	3.3V Linear 3.96A
5VDUAL1	-	5V Switch 4.85A
5VDIMM	-	5V Switch 8.29A

DDRII x2 & TERMINATOR		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	4.7A
1.8V VCC_DDR (S3)	-	400mA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

AGP Extender riser slot			
	HK4B	Luner Bear	
+12V	- 1A	- 1A	
+5V	- 5.0A	- 5.0A	
+3.3Vaux	- 2.28A	- 750mA	
+3.3V	- 11.6A	- 10.6A	
V_1P5_ICH	- 0.5A		

PCI_E x1 slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	3.0A

PCI slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	7.6A
+5V	-	5.0A

Card Board		
+3.3Vaux	-	1.2A

SPDIF Board		
+3.3V	-	1A
+3.3Vaux	-	0.33A
V_1P5_ICH	-	0.5A

USB x 9		
+5V (S0,S1)	-	4.5A
+5V (S3)	-	20mA


PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

5VAudio		
+5VR	-	500mA

+12V		
ATX	-	2x2

+5V	+3.3V	+5VSB	+12V
24.97A			
ATX POWER			

3V		
Battery	-	

 MICRO-START INTL CO.,LTD.		
Title		
POWER DELIVERY		
Size	Document Number	Rev
	MS-7415	0B
Date:	Thursday, December 20, 2007	Sheet 31 of 32

L2B-0A change from LB-11 : (2007/11/07)

- Page6.
- * Change the vender of clock generator from CY505YC64Tto ICS9LP505-1HGLF.
 - * Remove C148 for RAID clock.
 - * Pull up PCICLK2 to VCC3 through R132 for overclocking of CPU and SRC NOT allowed.
 - * Add C23/C24 for 6 power pin(VDD_CLK_IO) by vender request.

- Page14.
- * Remove off-page connector of PGNT2# for VT6410.

- Page15.
- * Add JCI1 for GPIO33. (Intel recommend).
 - * Add the net of STAT4 from ICH.
 - * Change the detect pin of clear password form SIO- INTRUDER to ICH9-GPI56.
 - * Add GPO16(FAN_SW) for CPU_FAN1&2 detection circuit.
 - * Remove off-page connector of HWM_INT.
 - * Remove off-page connector of GPIO13.
 - * Remove off-page connector of IO_SMI and generate IO_SMI through "SERIRQ" instead of using IO_SMI# pin from SMSC5617.

- Page17.
- * Add 1 SATA connector(SATA3_White). (NECP request)

- Page19.
- * Change this page from "IDE VT6410"to "FAN control/Detect".
 - * Remove all of VT6410 circuit from original page19 of LB schematic.
 - * Add switch circuit of FANTACT for CPUFAN1&CPUFAN2.

- Page21.
- * Change the type of SIO from SMSC5017 to SMSC5617.

- Page25.
- * Remove D5&net IDEACTP# from schematic.(For IDE LED)
 - * Add EMI capacitances C32/C36/C38/C49/C71.

- Page26.
- * Remove R352&C356&net PCIRST#2 for VT6410 PCI_RST# form schematic.

- Page29.
- * Add 1 jumper cap for JCI1.
 - * Change PCB from 7400-1.1 to 7415-0A.

L2B-0B : (2007/12/19)

- Page15.
- * Reserve R88 to keep only one system host on PECl bus.
 - * Add D5 for VBAT1.

- Page19.
- * Remove R452&R454 for fan switch(FANTACH1&2) circuit.

- Page21.
- * Change the power source of SIO's Vbat pin from VBAT to VBAT1.

- Page17/23/25.
- * Add EMI capacitance : C115, C143, C118, C373, C404, C628, C606, C642.